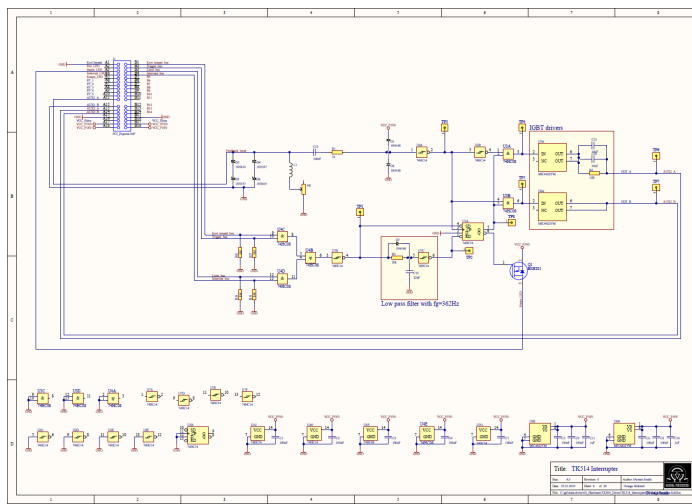
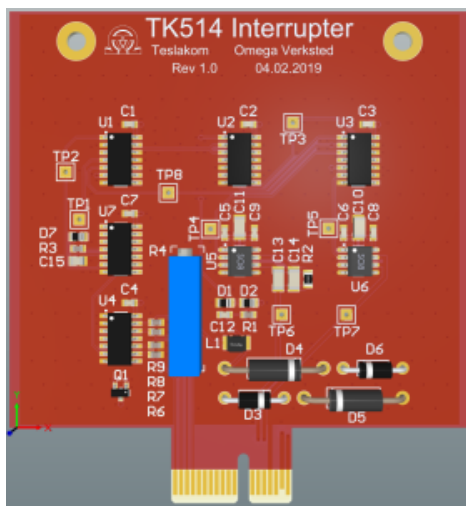


TK514 Interrupter

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Teori

Bakgrunn

TBD

Virkemåte

The interrupter generates the signal which drives the resonant circuit (coil rig) at its resonant frequency f_0 . As long as the input signal X2 is high the output produces a square wave with fundamental frequency f_0 . It does this by means of a positive feedback loop. The feedback signal X8 is retrieved with a sensing transformer around the output wire from the power amplifier (section 2.4), before being clamped, rectified, and schmidt triggered. This results in a cleaned up normalized representation of X8, lets call this signal X80. The flanks of X80 represents when the output current passes zero (this is when we want to switch the polarity of the output X5). X80 is fed to the output via gates controlled by a latch. X5_B is inverted in relation to X5_A (for push-pull operation). This circuit is shown in fig. 2.5. U1A is the latch which is central to the operation of the interrupter. It has Four inputs SD, CP, D, and RD, which are 'Set Data' (active low), 'Clock Pulse', 'Data', and 'Reset Data' (active low) respectively. And two outputs; Q which is the normal output, and Q inverted which is the inverted of Q at all times, Q inverted is unused in this circuit.

	Device	t_{pd} Typ (ns)	t_{pd} Max (ns)
t_{inv}	74HC14	12	25
t_{and}	74HC08	10	20
t_{drivR}	MIC4422YM Rising	20	80
t_{drivF}	MIC4422YM Falling	40	80

Table 2.1: Propagation delays for devices

	$T_J = 25^\circ C$	$T_J = 150^\circ C$
Turn-On Delay Time (ns)	46	31
Turn-Off Delay Time (ns)	120	210

Table 2.2: Turn on and off delays in the IGBT IRG4PC50WPbF

$$\overline{t_{pd}} = t_{inv} + \frac{t_{inv}}{2} + t_{and} + \frac{t_{drivR} + t_{drivF}}{2} \quad (2.1)$$

In addition the delays from hysteresis in U2A t_h and switching delays in the transistors in the power amplifier t_{sw} should be added to the desired phase lead t_d . Resulting in the desired phase lead t_d being given by eq. (2.2).

$$t_d = t_h + \overline{t_{pd}} + t_{sw} \quad (2.2)$$

The feedback signal X8 should have sufficiently high voltage so that delays from hysteresis t_h in U2A is negligible. Delays in the IGBT is read from the datasheet and presented in table 2.2. If we add the delay at 25 C to the nominal t_d and the delay at 150C to the maximum t_d , we get a t_d of 141 ns nominal and 258 ns maximum. Since there are no other resistances in the circuit than R2, as R1 is in series with both a capacitor and the input of the logic gate U2A and can be considered close to infinite in relation to R2, the phase angle is given by eq. (2.3).

$$\theta = \tan^{-1} \frac{X_{L1}}{R_2} = \tan^{-1} \frac{\omega L_1}{R_2} = \tan^{-1} \frac{2\pi f_0 L_1}{R_2} \quad (2.3)$$

And thus the desired phase lead is given by eq. (2.4), and the relation between L1 and R2 is given by eq. (2.5).

$$t_d = \frac{\theta}{\omega} = \frac{\theta}{2\pi f_0} \quad (2.4)$$

$$\frac{L_1}{R_2} = \frac{\tan(\theta)}{\omega} = \frac{\tan(\omega t_d)}{\omega} = \frac{\tan(2\pi f_0 t_d)}{2\pi f_0} \quad (2.5)$$

Given $f_0 = 110\text{kHz}$ and desired $t_d = 141\text{ ns}$ nominal and 258 ns maximum we get $L/R = 1; 4\ 107\text{ s}$ nominal and $L/R = 2; 6\ 107\text{ s}$ maximum. The total magnitude $|Z_L|$ of the impedance Z_L of L1 and R2 should give a sufficiently high voltage U_{X8} so that the delay due to hysteresis in U2A is negligible, but not too high voltage for the zener diodes D3-D6 to handle. The equation for $|Z_L|$ is shown in eq. (2.6).

$$|Z_L| = \sqrt{R_2^2 + (2\pi f_0 L_1)^2} \quad (2.6)$$

The relation between the peak voltage $|U_{X8}|$ over R_2 and L_1 is shown in eq. (2.7) assuming X_8 is sinusoidal.

$$|U_{X8}| = |Z_L| |I_{X6}| \frac{n_1}{n_2} \quad (2.7)$$

Reset network

The function of the network connected to the reset (RD) of the latch (U1A) is to reset the latch after a delay in the case that a zero crossing is not detected on X_8 after X_2 goes low. Note the inverting schmitt triggers U2C and U2D on both sides of the network. When X_2 goes high the input of U2D goes low immediately due to the capacitor C2 being discharged through D7, but when X_2 goes low the capacitor C2 will be charged through R3 and there will be a delay before the latch is reset. The time constant of R3 C2 is $\tau = 440 \text{ } 106\text{s}$, the positive going threshold voltage of the inverting schmitt trigger (74HC14) is $V_{T+} = 2.5\text{V}$ which is half of the supply voltage V_{CC_P5V0} . We know that a capacitor is charged to $0.5 V_{CC}$ (where V_{CC} is the applied voltage) after 0.7τ , thus the filter R3 C2 together with U2D introduces a delay of $0.7 \tau = 308\text{s}$, or if we have a resonance frequency f_0 of 110 kHz a delay of about 3.4 periods $T = 1/f_0$. If the synchronous shutdown does not work properly this filter should prevent or reduce noise from the interrupter not shutting down properly between each pulse on the input signal X_2 . This can also reduce the spark length if the spark is prevented from unintentionally continue longer than intended.

Input clamping and protection

D3-D6 are protection diodes which clamp the feedback signal to safe voltages. The network L1 and R2 introduces a tunable phase lead on the voltage. C1 and R1 is a filter to remove noise. D1 and D2 clamps the voltage to 0-5V.

IGBT Drivers

U5A and U6A are transistor drivers which amplify X_4 and step up the voltage from 5V to 18V

External resources:

https://www.stevehv.4hv.org/new_driver.html

Spec

Interruptindikator for alle slemme interrupts

Separat indikator for signalinterrupt



TK514_Interrupter.PDF

Versjoner

V0.0 (2009)

Changelog

1. Laget av Dewald De Bruyn

Errata

1. Ingen

V0.1 (2014)

Changelog

1. Kopt fra 2009 design

Errata

1. Ingen

V1.0

Release: 2017-03-16

Antall: 10

Changelog

1. Bakplanifisert
2. Lagt til testpunkter
3. Lagt til (footprint for) potmeter og spole R4, L1 for å kunne justere phase lead

Errata

1. Mangler thermals på jordpinner.
2. C10 og C11 kan "krympes" til 0805
3. C15 kan krympes til 0603
4. D1, D2, D7 kan krympes til 0603

Produserte kort

[illegible]